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(71) Applicant: **NOKIA MOBILE PHONES LTD.**
02150 Espoo (FI)

(72) Inventor: **Järvinen, Esko**
02360 Espoo (FI)

(74) Representative: **Johansson, Folke Anders et al**
Nokia Corporation,
P.O. Box 319
00045 Nokia Group (FI)

(54) Radio frequency amplifiers

(57) A radio frequency amplifier having a power transistor (Q1) to the base of which is coupled a radio frequency signal to be amplified. An amplified radio frequency signal is provided at the collector of the power transistor (Q1). A control transistor (Qc) has its base coupled to the base of the power transistor (Q1) whilst a driver transistor (Q2) provides a control bias signal to the bases of the control and power transistors. A differential amplifier (Qd1, Qd2) has a first input coupled to an input bias signal and an output coupled to the base of the driver transistor (Q2). The collector of the control transistor (Qc) is coupled to a second input of the differential amplifier to provide a negative feedback signal to the differential amplifier and the driver transistor (Q2) and thereby to stabilise the operating point of the power transistor (Q1).

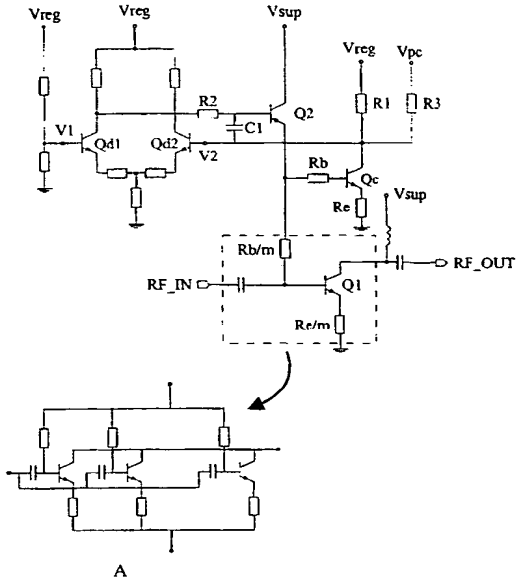

Figure 3

EP 0 942 524 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 66 0036

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 532 648 A (CULLING DENNIS A) 2 July 1996 (1996-07-02) * column 3, line 32 - column 4, line 19; figures 3,4 *	1,9	H03F1/30 H03G1/04
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 344 (E-0955), 25 July 1990 (1990-07-25) & JP 02 116203 A (MITSUBISHI ELECTRIC CORP), 27 April 1990 (1990-04-27) * abstract *	1,9	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03F
H03G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 January 2001	Blaas, D-L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 66 0036

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(71) Applicant : **SGS-THOMSON MICROELECTRONICS, INC.**
1310 Electronics Drive
Carrollton Texas 75006 (US)

(72) Inventor : **Rotay, Craig J.**
629 Franklin Street
Lansdale, Pennsylvania 19446 (US)

(74) Representative : **Palmer, Roger et al**
PAGE, WHITE & FARRER 54 Doughty Street
London WC1N 2LS (GB)

(54) Device for biasing an RF device operating in quasi-linear modes with temperature compensation.

(57) A biasing device which is in thermal contact with an RF device for actively biasing the RF device operating in quasi-linear modes. The biasing device provides a low impedance current source with high current capability to the base of the RF device. The biasing device includes three specially-processed transistors. The second and third transistors are connected such that their base-emitter and base-collector junctions are in parallel effectively forming two exceptionally low turn on series diodes. The result of reducing the resistances of the second and third transistors, by configuration and processing, is that they turn on slightly before the RF device is biased to its quiescent point.

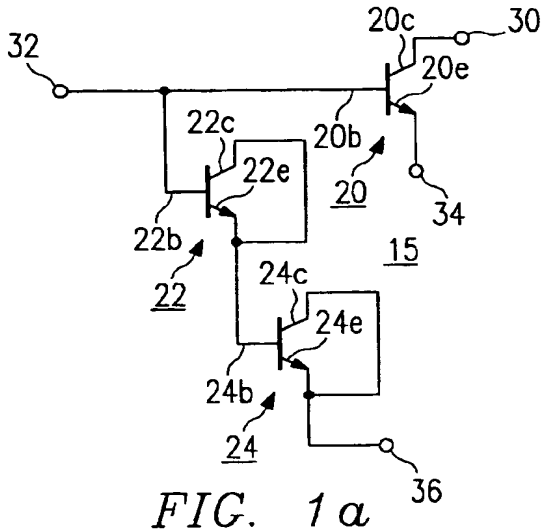

FIG. 1a

EP 0 583 991 A1

The present invention relates generally to a device for biasing an RF device and, more particularly, to a single-package integrated circuit device using specially-processed transistors for biasing an RF device operating in quasi-linear modes.

It is well-known that RF devices operating in quasi-linear modes require biasing circuitry. In these modes, effective biasing circuitry should supply the RF device with its current requirements while accounting for drifts in the RF device's operating point due to temperature variations. If uncontrolled, the drifting due to temperature may lead to catastrophic device failure (i.e., "thermal runaway").

Thus, the effectiveness of a biasing device is related to its current supply capability, its internal resistance (which also affects it current supply capability) and its ability to prevent thermal runaway (caused by uncontrolled drifting of the operating point). Additional considerations for determining the usefulness and appeal of a biasing device include the amount of space it consumes, the need for support devices, and the effects on total amplifier efficiency, linearity, stability and reliability.

Traditional biasing techniques such as resistive voltage division, diode bias or bypassed emitter bias can no longer satisfy the aggressive specifications imposed on RF transistors without substantial reduction in total system efficiency and/or common-emitter power gain. These techniques also tend to degrade (or limit) the linearity and dynamic range of the RF device under test.

A biasing device being in thermal contact with an RF device for actively biasing the RF device operating in quasi-linear modes. The biasing device provides a low impedance current source with high current capability to the base of the RF device. The biasing device includes three transistors. The base of the second transistor is connected to the base of the first transistor and the collector of the second transistor is connected to the emitter of the second transistor for reducing the resistance. The base of the third transistor is connected to the emitter of the second transistor and the collector of the third transistor is connected to the emitter of the third transistor for reducing the resistance. The result of reducing resistances of the second and third transistors is that they turn on slightly before the RF device is biased to its quiescent point.

The invention is best understood from the following detailed description when read in connection with the accompanying drawings, in which:

Fig. 1a is a circuit diagram of a biasing device in its basic configuration;

Fig. 1b is a schematic representation of Fig. 1a;

Fig. 2 is an illustration of the diamond matrix architecture used for processing one of the transistors in Fig. 1a;

Fig. 3 is an illustration of the interdigitated architecture used for processing two of the transistors in Fig. 1a;

Fig. 4a shows an isometric view of the circuit board on which the biasing device and an RF device will be mounted;

Fig. 4b shows a side view of Fig. 4a with arrows representing thermal transfer from the location of the RF device to the location of the biasing device;

Fig. 5 shows the biasing device of Fig. 1a connected to an RF device for biasing purposes;

Fig. 6a shows a temperature versus voltage performance graph for the biasing device of Fig. 5;

Fig. 6b shows a the quiescent current supplied to the RF device during the conditions shown in Fig. 6a;

Fig. 6c shows a comparison between the base-to-emitter characteristic curve of a compensating transistor (diode) versus that of a standard RF device for high current;

Fig. 6d shows a similar comparison to Fig. 6c at low current, exemplifying the mirror-like tracking ability of the biasing device;

Fig. 7a shows the biasing device of Fig. 1a in its basic configuration;

Fig. 7b shows an alternate embodiment of the biasing device in Fig. 7a modified to protect against a reverse voltage;

Fig. 7c shows an alternate embodiment of the biasing device in Fig. 7a modified to provide more power output;

Fig. 7d shows an alternate embodiment of the biasing device in Fig. 7a modified to provide push-pull or dual-stage operation;

Fig. 7e shows an alternate embodiment of the biasing device in Fig. 7a modified for higher overall efficiency and sensitivity;

A. Definitions

Within this specification, the following terms or phrases have the corresponding definitions:

RF device. RF NPN Bipolar Transistor

Quasi-linear modes. Modes of operation during which the conduction angle in a cdmmon emitter configuration falls at or between 180° and 360°. These modes are generally referred to as classes AB_1, AB_2 and B.

B. Overview

Biasing device 15, as shown in Fig. 1a, is a single package integrated circuit (IC) consisting of three specially-processed transistors. Biasing device 15 provides an exceptionally low-impedance current source with superior thermal tracking for an RF device operating in quasi-linear modes.

Biasing device 15 is capable of supplying a range

of current (from nanoAmperes to Amperes) to the base connection of an RF device without adversely affecting its ability to track the base-emitter voltage (V_{be}) of the RF device. Some potential adverse effects, which have been minimized by the chosen architectures and specially-processing the transistors in the biasing device 15, typically arise from a transistor's internal resistance which can not only limit its current capabilities but also distort (relative to those of the RF device) the turn-on characteristics of the compensating transistors.

Biasing device 15 provides this range of current while accurately tracking changes in the RF device's V_{be} with respect to temperature. Voltage changes occur due to an intrinsic characteristic of all silicon PN junctions, varying only slightly from device type to device type, which is that the PN junction voltage decreases by 2 to 2.5 millivolts per increase of 1° C. The changing V_{be} causes the operating point of the RF device to drift and, if inaccurately tracked by the biasing device, will likely cause the RF device to enter thermal runaway leading to catastrophic device failure.

Thus, to prevent thermal runaway, the biasing device 15 employs an active biasing technique capable of accurately tracking the change in V_{be} (with temperature) for the RF device while satisfying the RF device's current requirements in both switching and non-switching modes.

For a non-switching RF device, thermal runaway occurs if the base bias supply voltage to the RF device remains constant as the base-emitter junction potential decreases in response to increasing temperature. As the junction potential difference decreases, increasing collector current for the RF device is allowed to flow which is dictated by the increasingly over-driven base. A cycle is created as the increased collector current causes the junction temperature to rise, and, correspondingly, the base is effectively over-driven as a result of the constant base bias supply voltage. The cycle allows the collector current to increase exponentially. Eventually, high fusion currents destroy the device, thus, ending the cycle.

For a switching RF device, the above description applies with some additional concerns. First, the biasing device should have a sufficiently low source impedance in order to source-high levels of base current (which increases with increasing RF drive levels) without losing regulation of the RF BJT's bias point.

Second, the biasing device must sense changes in the RF device's junction temperature, and compensate for the change in the V_{be} at any point during the RF cycle, as well as during changes in the RF signal's amplitude.

And, third, the biasing device can not be susceptible to the rectification effects of the RF BJT's base-emitter junction during which the negative voltage developed opposes the positive bias voltage which tends to lower the bias point of the RF device.

Accurately tracking the base-emitter voltage of an RF device while providing a low impedance current source are important features to designers requiring maximum linear performance, stability, easy-to-control operating points, overall quasi-linear amplifier reliability and high system efficiency. In addition to these desirable properties, due to its processing and packaging, the biasing device requires minimal board space and a minimal number of support devices.

B. Construction

As seen in Fig. 1a, in its basic configuration, biasing device 15 comprises three transistors, 20, 22 and 24. Transistors 22 and 24 are connected in series and are the compensating transistors. In the exemplary embodiment of biasing device 15, all connections between transistors are made using 0.002" O.D. gold wire.

Collector 22c is directly connected to emitter 22e of transistor 22. And, emitter 22e, along with collector 22c, of transistor 22 is directly connected to base 24b of transistor 24. Similarly, collector 24c is directly connected to emitter 24e of transistor 24.

Directly connecting collectors 22c and 24c of the two transistors to their respective emitters 22e and 24e, along with certain processing features described below, effectively results in two exceptionally low turn-on series diodes 26 and 28 (see Fig. 1b). Thus, by reducing the resistance of each effective series diode 26 and 28, a characteristic curve, as seen in Figs. 6c and 6d, for each diode can be achieved that mirrors the characteristics of the RF device yet at lower voltages.

The relationship illustrated in Figs. 6c and 6d is advantageous because diodes 26 and 28 turn on at a voltage slightly less than the voltage needed to bias an RF device to its quiescent level. As seen in Figs. 6c and 6d, the voltage difference is approximately 0.05 to 0.1 volts. This ensures that both devices, the biasing device 15 and the RF device, are operating at mirroring points along their turn-on curves simultaneously. The difference between the two curves is the result of the compensating transistor, 22 and 24, being situated at two stages of gain prior to the RF device, and is a key feature to the overall performance of biasing device 15.

Collector 20c is connected to terminal node 30. Base 20b and base 22b are both connected to terminal node 32. Emitter 20 leads to terminal node 34, and emitter 24e leads to terminal node 36. Terminal nodes 30, 32, 34 and 36 are connected, via gold wires, to the IC's package leads, hence, they are externally accessible.

Base 22b and emitter 22e, in parallel with base 22b and collector 22c, form the first PN junction, having an approximate forward bias breakdown voltage of .7v (Vfbe). Base 24b and emitter 24e, in parallel

with base 24b and collector 24c, form the second PN junction, also having an approximate forward bias breakdown voltage of .7v. Thus, the total voltage drop from base 22b to emitter 24e is approximately 1.4v. It should be noted that the total voltage drop is actually slightly lower due to the lowered resistance of the devices stemming from the paralleled junction configuration and certain processing techniques.

Because paralleled junctions of transistors 22 and 24 are used, the circuit in Fig. 1a can be schematically represented as in Fig. 1b where the parallel junctions of transistor 22 correspond to diode 26 and the parallel junctions of transistor 24 correspond to diode 28.

In the exemplary embodiment of biasing device 15, transistor 20 is specially-processed and selected for suitable operation in an emitter-follower configuration having extremely low source impedance, as required by an ideal current source. Transistor 20 has an internal resistance of approximately 100 milliohms and an H_{fe} of 35.

The top level mask of transistor 20 employs a conventional diamond matrix architecture, as seen in Fig. 2, and consists of refractory gold metallization and large bond pad areas for gold wirebonding. Bonding areas are designated by "E" for emitter connections and "B" for base connections. The collector connection for this type of RF transistor is the entire underside (not shown) which consists of a barrier metal layer of tungsten which allows gold to be plated to the wafer. The two step process involves high voltage sputtering of the barrier metal onto the silicon substrate, which prevents the highly porous gold backside from diffusing into the silicon, thus, destroying previously created junctions. The gold is then electroplated to barrier metal using standard techniques. The backside gold metallization allows the completed transistor die to be eutectically attached to the gold metallization within the package.

The above metallization steps follow numerous processing steps involving photolithography techniques to develop base and emitter regions from layer masks onto the starting substrate (N type collector region). This is accomplished by exposing photoresist which allows particular areas to remain while others are etched away. The layer masks are used in sequence to form base and emitter regions, where, after etching, a P or N type dopant (respectively) is introduced at specific levels of concentration. After contacts to the base and emitter regions through insulating barriers of oxide are formed, connections to the top metal layers complete the fabrication of the transistors. These apply to both NPN and PNP BJT's; however, the exemplary embodiment of biasing device 15 involves NPN BJT's.

Some distinguishing characteristics of biasing device 15 are inherent in the geometry of transistor 20, while others are introduced at specific points during fabrication of transistors 20, 22 and 24. The geometry of transistor 20, was chosen for its high emitter periphery, specifically for the high number of base-emitter junctions throughout the chip, which provides low source impedance and, consequently, high current capability.

Additionally, the diffusion of the emitter into the base region was specifically processed for a low forward voltage drop (V_{fbe}) which further lowers the impedance by reducing the junction's internal resistance. Also, the base diffusion for this die type is exceptionally large (i.e., high base area) and has a wide depletion region. This translates into inherent stability even at low frequencies by reducing the likelihood of oscillations, as well as lowering the H_{fe} which allows for a greater margin of error when adjusting biasing device 15 to properly bias an RF device.

Finally, the substrate (starting material) of transistor 20 contains thick, high resistivity epitaxial layers which give the collector region a high breakdown voltage. This decreases the collector to emitter leakages (which tend to forward bias the RF transistor), thus extending the operating voltage range of biasing device 15. In fact, the breakdown voltage is high enough to allow biasing device 15 to operate at the normal operating voltages of today's linear RF transistors. This affords advantages in both reliability and versatility.

In the exemplary embodiment of biasing device 15, the fabrication of transistors 22 and 24 is similar to that of transistor 20 except as described below.

The top level masks of transistors 22 and 24 employ a conventional interdigitated architecture as seen in Fig. 3. The geometry of transistors 22 and 24 has been chosen for its thermal tracking capability. Because this architecture mimics that used in standard RF devices, the ability of compensating transistors 22 and 24 to compensate for an RF device is inherently enhanced.

This occurs for several reasons. First, the interdigitated geometry is dense and symmetrical which is critical to proper current sharing which, in turn, is necessary for optimal compensation.

Second, because the base and emitter regions of transistors 22 and 24 are geometrically the same as those of a standard RF device, the base-emitter characteristic curves of transistors 22 and 24 will closely resemble those of a given RF device.

Third, the intentional polysilicon emitter ballast (or internal resistance) for transistors 22 and 24 is processed using the same techniques used for standard RF devices, although the level of the total junction resistance for transistors 22 and 24 is lower for reasons described below.

The geometry chosen for transistors 22 and 24 also incorporates a large number of active areas having high quantities of base and emitter fingers. The fingers significantly increase the emitter periphery

and, when coupled with the paralleled junctions, increases the current handling capability, thereby extending the useful operating range of biasing device 15.

In addition to the geometry, certain processing modifications for transistors 22 and 24 are important to achieve optimal compensation characteristics.

First, the processing begins with lower resistivity starting material (lower relative to transistor 20) translating to lower junction breakdown voltages. This means that the junctions, in particular the base-emitter, of transistors 22 and 24 behave similarly to those of a standard RF device, but will generally begin to breakdown at slightly lower voltages.

Additionally, the emitter resistance of transistors 22 and 24 is intentionally lowered during the ballast processing step to further ensure lower-voltage turn on characteristics. This is accomplished by using the lowest ballasting necessary to promote equal current sharing between active areas.

Finally, because transistors 22 and 24 are connected (as previously discussed) in such a way that the base-collector junctions are in parallel with the base-emitter junctions (effectively forming two very low turn-on series diodes 26, 28), normal transistor action ceases. This means that the H_{fe} of transistors 22 and 24 is no longer a concern, hence, allowing for much simpler ion implantations of dopant into the base and emitter regions during processing. This significantly improves high overall device yields.

The low turn-on characteristic of the effective series diodes 26 and 28 is important for proper compensation of an RF device. The bias voltage which is related to the base bias current supplied by biasing device 15 to the RF device will likely be greater than the bias voltage at the base of transistor 20, due to the H_{fe} associated with transistor 20. Thus, the low voltage turn-on of the series diodes 26 and 28 allows them to track the RF device's turn-on characteristic curve at a proportionally lower voltage, as seen in Figs. 6c and 6d. This ensures that diodes 26 and 28 are fully turned on by the time the RF device is biased at higher quiescent levels, thereby providing linear compensation of the [delta]V_{be} within an RF device at all operating points.

Additionally, this allows biasing device 15 to properly track the I_{cq} point even with extremely low bias levels such as those in class B mode where the RF device is biased at cutoff.

The above features offer enhancements in all major performance areas, for instance, linearity and intermodulation distortion, stage gain, and amplifier stability. Because biasing device 15 is designed for low current consumption, especially when compared to other transistor biasing techniques, system efficiency can dramatically increase.

Biasing device 15 is provided in a single package. Since efficient tracking of the biasing device 15 depends on accurately sensing the temperature of the RF device, the package should be thermally conductive. Additionally, the package should be positioned in the same thermal plane and, preferably, in close proximity to the RF device (in the exemplary embodiment of a biasing device 15, this distance is approximately within 2-3 inches of the RF device). Fig. 4a shows the thermally conductive mounting plane 41 indicating the locations 37, 39 at which both the biasing device 15 and RF device are secured, respectively. Fig. 4b, using arrows, illustrates the thermal transfer from the location 39 of the RF device to the location 37 of biasing device 15.

It should be noted that the closer the biasing device 15 is positioned relative to the RF device, the faster it can compensate due to the changes in temperature and voltage. More particularly, thermal transfer over an increasingly large distance results in an increasing thermal time constant, which adds to the time it takes biasing device 15 to compensate within the thermal feedback loop. This means that the adjustment in bias point will not be a linear function with respect to temperature, but, instead, a distantly placed biasing device 15 will likely under-compensate while the RF device heats up and over-compensate as the RF device cools down. This is known as thermal hysteresis. Thus the goal is to linearize the hysteresis characteristic by minimizing the distance between biasing device 15 and the RF device, thus reducing the thermal time constant.

In the exemplary embodiment of biasing device 15, the package includes a thermally conductive copper base and/or flange and a non-hermetically sealed ceramic lid. Also, the footprint of the package should be sufficiently large in area such that adequate thermal conductivity occurs.

C. Use and Operation

In use, continuing with Fig. 1a, the terminal node connections 30, 32, 34 and 36 are used in the following way:

Terminal node 30 is the positive voltage supply (+Vce). In the exemplary embodiment of a biasing device 15, terminal node 30 is capable of being operated at any V_{ce} of the RF device from 5v to 50v. This is a significant increase in range relative to existing devices.

Terminal node 32 is the bias adjust voltage. The voltage at this node should be selected such that transistor 20 is forward biased. It should be noted that this is easily accomplished with a variable resistor in rheostat configuration; and, with simple computations, a fixed resistor can permanently set the bias point.

Terminal node 34 is the base bias voltage. This is the output of the biasing device 15 which provides a temperature compensated base voltage to the RF device with dynamic current capability. This voltage

is calculated by V_{fbe} - [delta]V_{be}.

Terminal node 36 is grounded (or connected to a third diode). Because the thermal tracking of the biasing device 15 is dependent on sensing the temperature of the RF device, the biasing device's position relative to the RF device is critical, requiring that it must be in close proximity. However, when this is physically impossible for mechanical reasons or otherwise, two more diodes may be added, external to the IC. The first diode is placed between transistor 20 and the RF device but in the same thermal plane as biasing device 15. It is this diode which now corresponds to and is compensated for by transistor 24. The second diode is placed between transistor 24 and ground but in the same thermal plane as the RF device. It is this diode which now corresponds to and compensates for the base-emitter junction of the RF device. This diode may be smaller and, therefore, easier to place near the RF device.

Fig. 5 shows an RF device connected, for biasing purposes, to biasing device 15. A variable resistor 40 is connected between terminal nodes 30 and 32. Emitter 20e of transistor 20 is connected to inductor 44a, which performs the function of an RF choke. Inductor 44a is then connected to base 42b of RF device 42. Collector 20c of transistor 20 is connected to V_{ce} as well as inductor 44b which also performs the function of an RF choke. Inductor 44b is then connected to collector 42c of RF device 42.

In operation, a user should select the appropriate value for resistor 40 such that RF device 42 is properly biased and an equilibrium is achieved with respect to temperature. Although there are numerous ways for calculating an appropriate value for resistor 40, a brief description of one possible method is provided:

To determine the appropriate value for resistor 40, the values for RF device's 42 quiescent current ($I_{cq\text{-}rf}$), the D.C. current gain ($H_{fe\text{-}rf}$) for RF device 42 and the D.C. current gain ($H_{fe\text{-}bd}$) for biasing device 15, and the source voltage (V_{ce}) are required.

Next, the base current ($I_{b\text{-}rf}$) for RF device 42 is calculated: ($I_{b\text{-}rf}$) = ($I_{cq\text{-}rf}$)/($H_{fe\text{-}rf}$). In the exemplary embodiment, ($I_{b\text{-}rf}$) is supplied by biasing device 15 at approximately 0.7v ($V_{be\text{-}rf}$).

Next, the base current ($I_{b\text{-}t20}$) for transistor 20 is calculated: ($I_{b\text{-}t20}$) = ($I_{b\text{-}rf}$)/($H_{fe\text{-}bd}$). In the exemplary embodiment, ($H_{fe\text{-}bd}$) is intentionally low (approximately 30 to 35) such that it is insensitive to varying ($H_{fe\text{-}rf}$) as well as forcing more controllable values of resistor 40.

Next, the current through the series diodes (I_{dio}) can be approximately ($I_{b\text{-}rf}$). This is due to the turn-on characteristics of the diodes and the RF device. Furthermore, an increasing (I_{dio}) ensures proper tracking of the bias voltage with temperature and allows a linear shift in bias point with increasing (or decreasing) RF drive levels. It should be noted that operating on the "knee" of the diode's turn-on characteristic results in degraded thermal tracking and non-linear ($V_{be\text{-}rf}$) voltages with respect to ($I_{b\text{-}rf}$). These effects can be seen conceptually. However, the special processing of compensating transistors 22 and 24 tends to minimize the (I_{dio}) of the biasing device, thus making (I_{dio})=($I_{b\text{-}rf}$) a possible yet rare occurrence. Additionally, operation on the "knee" of the characteristic curve of compensating transistors 22 and 24 is less crucial due to biasing device's 15 inherent tracking capabilities.

Next, (I_{adj}) is calculated: (I_{adj}) = (I_{dio}) + ($I_{b\text{-}t20}$). Then, the "on" resistance of the series diodes for quiescent conditions is calculated: (R_{dio}) = ($V_{be\text{-}dio}$)/(I_{dio}). In the exemplary embodiment, ($V_{be\text{-}dio}$) is approximately 1.4v.

Finally, the value for resistor 40 can be calculated: resistor 40 equals (R_{tot} - R_{dio}) where (R_{tot}) equals (V_{ce})/(I_{adj}), or resistor 40 equals ((V_{ce})-($V_{be\text{-}dio}$))/(I_{adj}).

It should be noted that these equations represent the theory of operation. Because most parameters are determined empirically, and change dynamically from various conditions and devices, the results obtained from these calculations are approximate values. In practice, the value of resistor 40 will likely range from 500 to 15000 Ohms. Furthermore, enhanced control is realized by the addition of a low value resistor from the V_{be} output of biasing device 15 to ground at the expense of some system efficiency. The increase in total biasing device current decreases the value of resistor 40, yet increases overall bias stability.

As RF device 42 begins to operate, its temperature increases. The temperature increase causes the base-emitter voltage of RF device 42 to decrease at a rate of 2 millivolts/° C. As the base-emitter voltage decreases, RF device 42 maintains its quiescent current requirements. If the voltage external to RF device 42 either is kept constant or inaccurately tracks the base-emitter voltage of RF device 42, the mismatch can create circumstances leading to thermal runaway as described earlier.

Because biasing device 15 is required to be in the same thermal plane as RF device 42, as the temperature increases, transistors 22 and 24 (theoretically compensating for transistor 20 and 42, respectively) also heat up. As their temperatures increase, their base-emitter voltages also drop at the same rate as those of transistor 20 and RF device 42. This corresponding decrease in voltage ensures that the base voltage external to RF device 42 tracks the internal base-emitter voltage, thus, preventing thermal runaway.

Additionally, as transistors 22 and 24 heat up, more current flows through them and less flows to the base of transistor 20. This lowering of base current to transistor 20 provides constant quiescent level of current flow to the base 42b of RF device 42; thus,

the current flow to RF device 42 is regulated by biasing device 15 by using the temperature of RF device 42 as an input parameter. It should be noted that resistor 40, acting in conjunction with transistors 22 and 24 as a voltage divider, somewhat restricts the flow of current from the source to the base of transistor 20.

It should be noted that, when biasing an RF device, proper bypassing and filtering techniques, well-known by those skilled in the art, should be used. Standard bypassing techniques are satisfactory for this circuit. Also, additional filtering should be considered when long lead lengths or connection runs are used.

As seen in Fig. 5, capacitors 46a and 46b provide filtering for the circuit. In the exemplary embodiment, each capacitor, 46a and 46b, is approximately .1 microF. High frequency bypassing is provided by capacitors 48a and 48b. And, D.C. block matching network is provided by 50a and 50b.

Figs. 6a and 6b show the performance of biasing device 15 in a non-switching state. Fig. 6a illustrates biasing device 15 ability to precisely track an RF device's base-emitter voltage due to temperature changes. And, Fig. 6b illustrates, while tracking the base-emitter voltage, biasing device 15 supplies the necessary quiescent current for proper biasing of the RF device under those conditions.

D. Alternate Embodiments

Figs. 7a through 7e show schematic diagrams of multiple embodiments in which the biasing device invention can be used. Fig. 7a shows the basic configuration of the biasing device 15, this embodiment is described above.

Fig. 7b shows a schematic diagram of a biasing device 15b which has two additional transistors 60 and 62. The purpose of transistor 60 is to provide reverse voltage protection. Terminal node 34 is connected to the collector of transistor 60 such that any voltage present at node 34 now travels through the collector-base junction of transistor 60 before reaching the emitter-base junction of transistor 20. Although this somewhat increases the source impedance, the collector-base breakdown voltage (approximately 50-70v) by far exceeds the emitter-base breakdown voltage (approximately 5v), thus, providing significant protection for the biasing circuit from a reverse voltage caused by a short-circuit or other unexpected condition.

It should be noted that because the base-collector junction is positioned between transistor 20 and an RF device, this junction needs to be compensated for by placing a base-collector junction after the two series diodes in order to ensure accurate thermal tracking and current regulation. As seen in Fig. 7b, this is done using transistor 62.

Fig. 7c shows a schematic diagram of biasing device 15c which has an additional transistor 20a in parallel with transistor 20 for the purpose of providing more power. The additional transistor 20a provides biasing device 15c with an additional power boost allowing it to provide approximately twice the power. Because the two transistors, 20 and 20a, are in parallel, there is no need, beyond the two transistors 22 and 24 (represented as diodes 26 and 28, respectively), to further compensate. The first transistor 22 can satisfactorily track and compensate for the parallel connection of the transistor's 20a base-emitter junction.

Fig. 7d shows a schematic diagram of biasing device 15d which has an additional transistor 21 and two additional diodes, 22a and 24a, for the purpose of providing a biasing device which can operate in a push-pull configuration. Essentially, this embodiment is two basic configurations side by side designed for allowing a single biasing device to regulate two sides of an RF device. It should be noted that each of the terminal nodes 32, 34 and 36, with the exception of terminal node 30, now has corresponding terminal nodes 32a, 34a and 36a. It should also be noted that because of the additional terminal nodes, if the biasing device 15d embodiment is to be used, a package with at least seven leads would be necessary.

Fig. 7e shows a schematic diagram of biasing device 15e which has an additional transistor 19, for the purpose of providing a biasing device which has enhanced efficiency and sensitivity. Essentially, this embodiment adds transistor 19 in a Darlington configuration with transistor 20 to enhance the sensitivity of the overall configuration. As is understood, the addition of transistor 19 into the basic configuration can also be done with the alternate embodiments seen in Figs. 7b through 7d for enhanced sensitivity.

Although the invention is illustrated and described herein embodied as a single-package integrated circuit for biasing an RF device operating in quasi-linear modes, the invention is nevertheless not intended to be limited to the details as shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the spirit of the invention.

Claims

1. A biasing device being in thermal contact with an RF device for actively biasing the base of the RF device operating in quasi-linear modes, said biasing device providing a source of low impedance current and high current capability, comprising:

   first, second and third transistors each having a collector, an emitter and a base;

   the base of said second transistor directly connected to the base of said first transistor, and the collector of said second transistor directly

connected to the emitter of said second transistor for reducing the resistance of said second transistor from base to emitter; and

the base of said third transistor directly connected to the emitter of said second transistor, and the collector of said third transistor directly connected to the emitter of said third transistor for reducing the resistance of said third transistor from base to emitter,

whereby said second and third transistors turn on at a voltage having a value slightly less than the voltage for biasing the RF device to its quiescent point.

2. The device of claim 1 wherein said first transistor has a diamond-matrix architecture.

3. The device of claim 2 wherein said second and said third transistors each have an interdigitated architecture.

4. The device of claim 3 wherein said second and said third transistors each have the lowest ballasting necessary for substantially equal current sharing between active areas.

5. The device of claim 4 wherein said second and said third transistors each use starting material with lower resistivity than said first transistor.

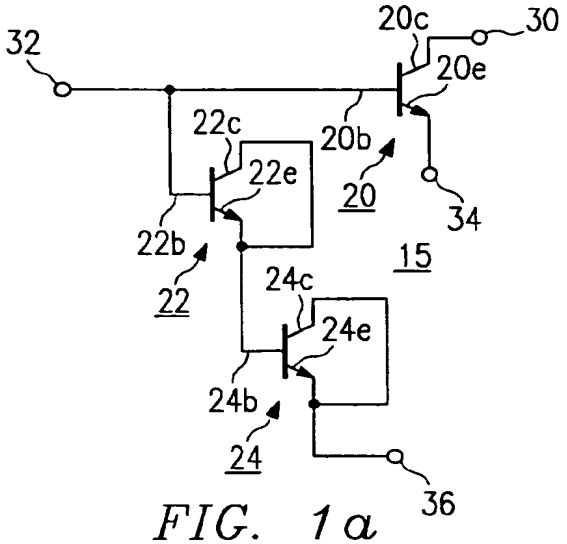

FIG. 1a

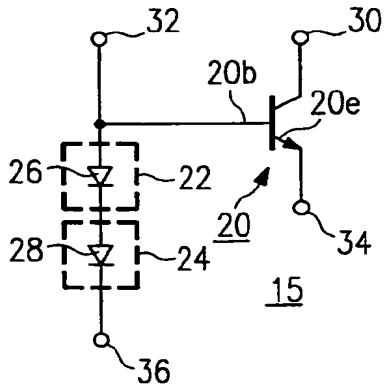

FIG. 1b

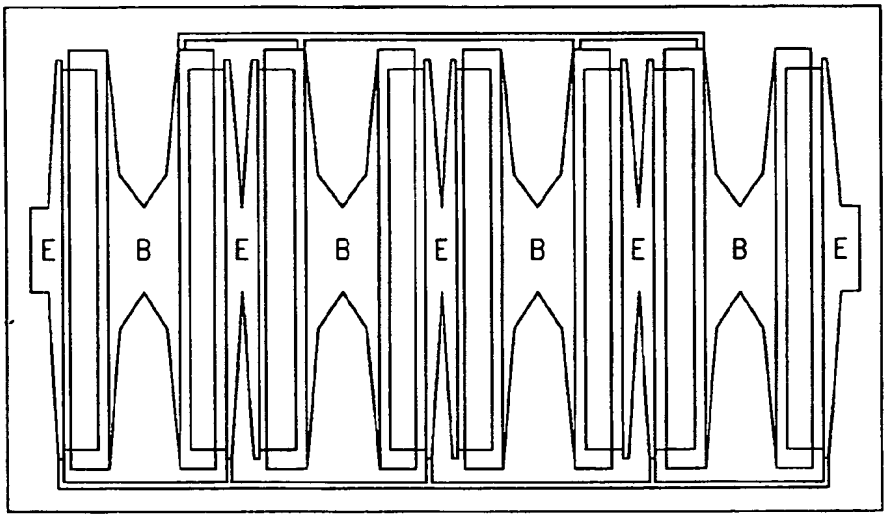

FIG. 2

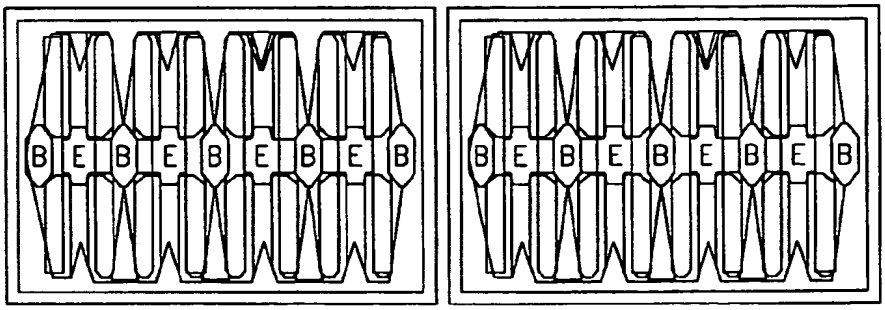

FIG. 3

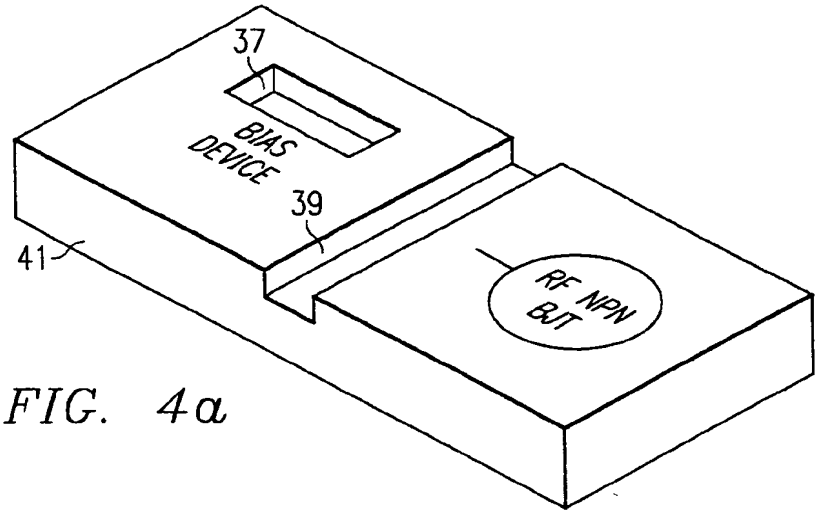

FIG. 4a

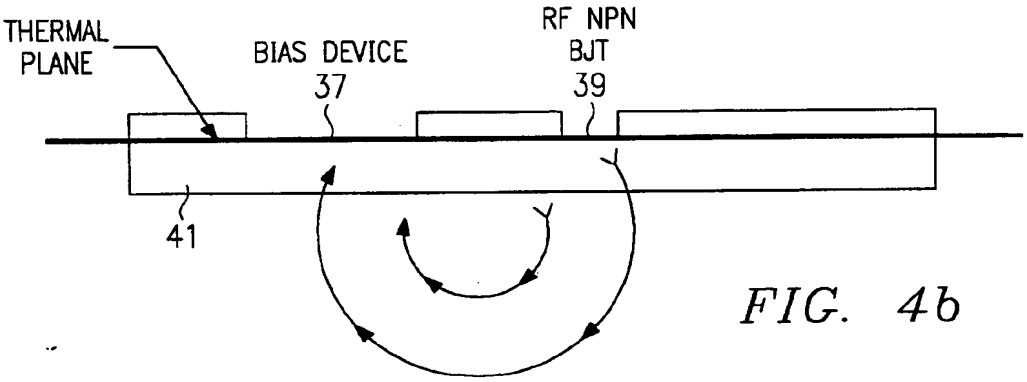

FIG. 4b

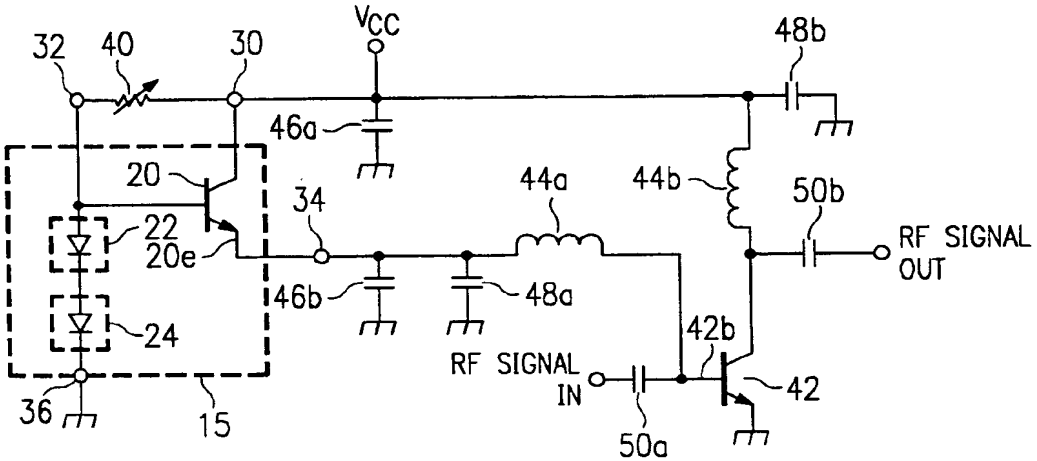

FIG. 5

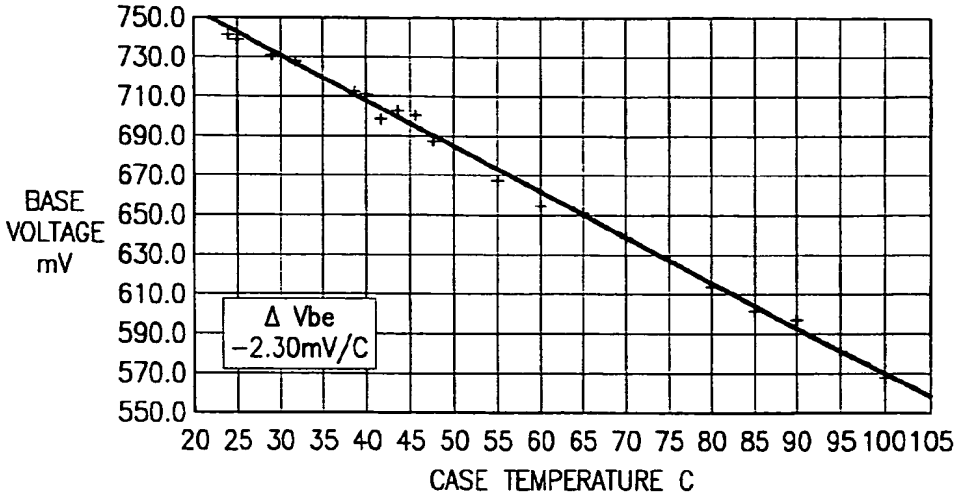

FIG. 6a

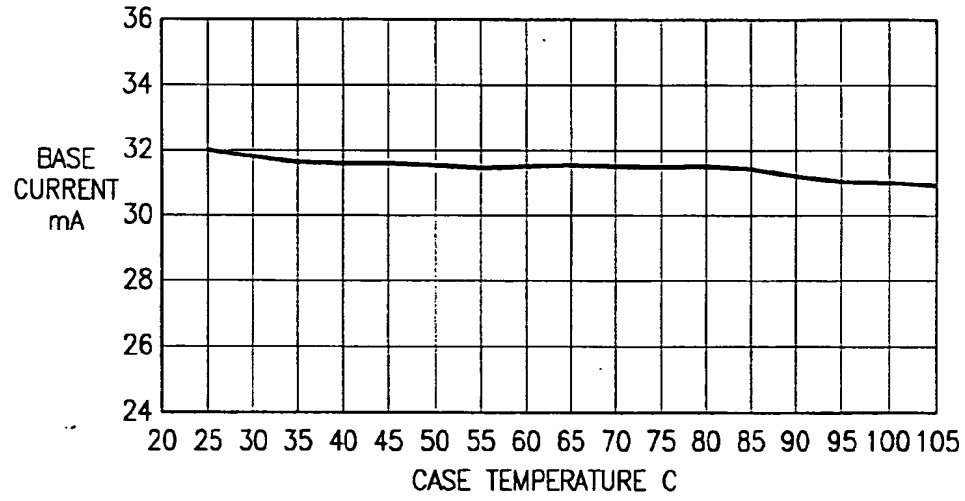

FIG. 6b

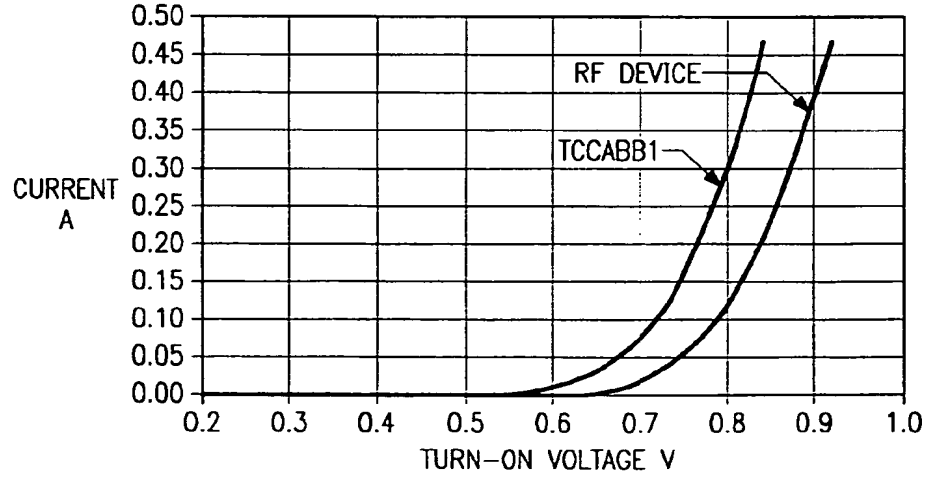

FIG. 6c

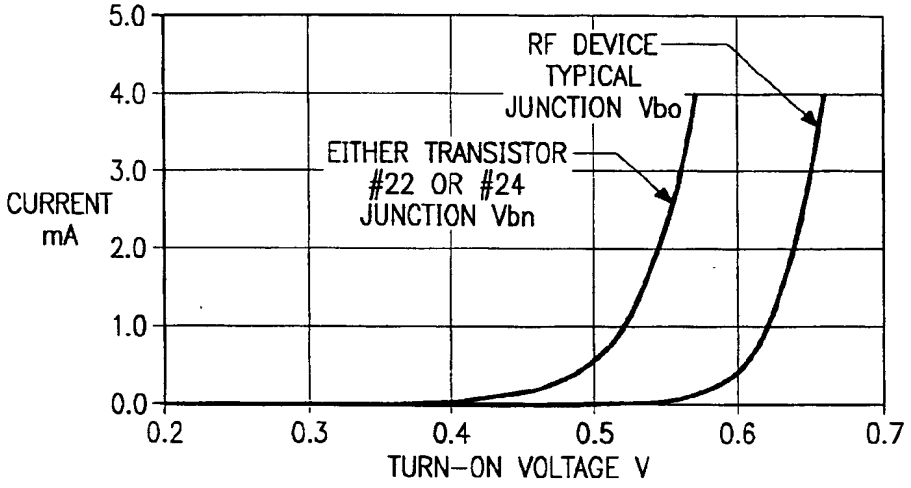

FIG. 6d

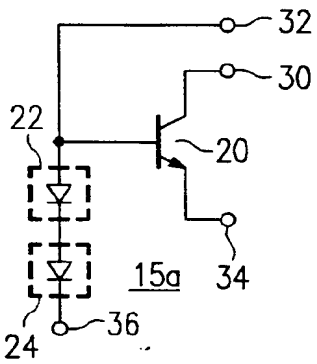

FIG. 7a

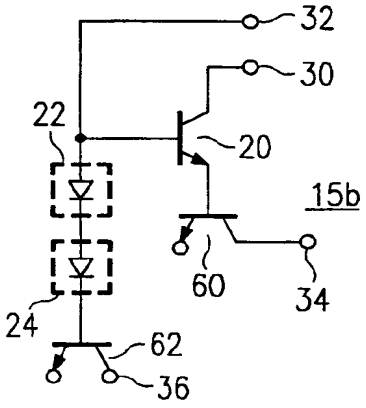

FIG. 7b

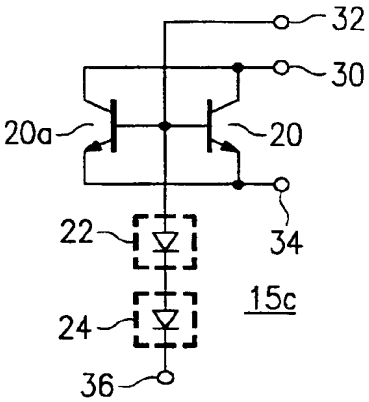

FIG. 7c

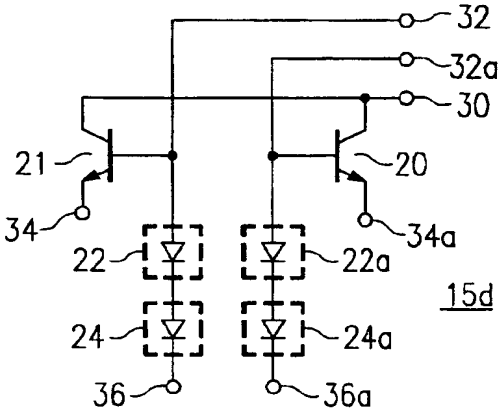

FIG. 7d

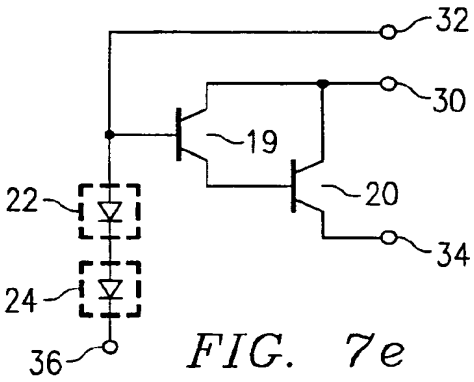

FIG. 7e

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 6576

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	US-A-4 924 194 (OPAS ET AL) * column 2, line 3 - column 3, line 9; figure 1 *	1	G05F3/22 H03F1/30
A	US-A-4 242 598 (JOHNSON ET AL) * column 3, line 38 - column 5, line 58; figures 5-9 *	1,3	
A	MOTOROLA TECHNICAL DISCLOSURE BULLETIN vol. 3, no. 1 , March 1983 , SCHAUMBURG, ILLINOIS, USA page 20 BOB GUNTHER 'LOW IMPEDANCE,TEMPERATURE COMPENSATED BIAS SUPPLY' * the whole document *	1	
A	US-A-4 320 349 (FREERS ET AL) * column 5, line 36 - column 6, line 9; figure 5 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

G05F
H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 November 1993	CLEARY, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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